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Data Acquisition Systems

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Outline

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DAS general architecture

Analog Section

- Characteristics
- Performance parameters

Digital Section

- Characteristics
- Signal processing basic concepts
- Sequential processing
- Block processing
- Performance parameters

A/D Section

- Performed transformations
- Components
- ADC general structure
- ADC main families
- Multichannel A/D Section
- Performance parameters

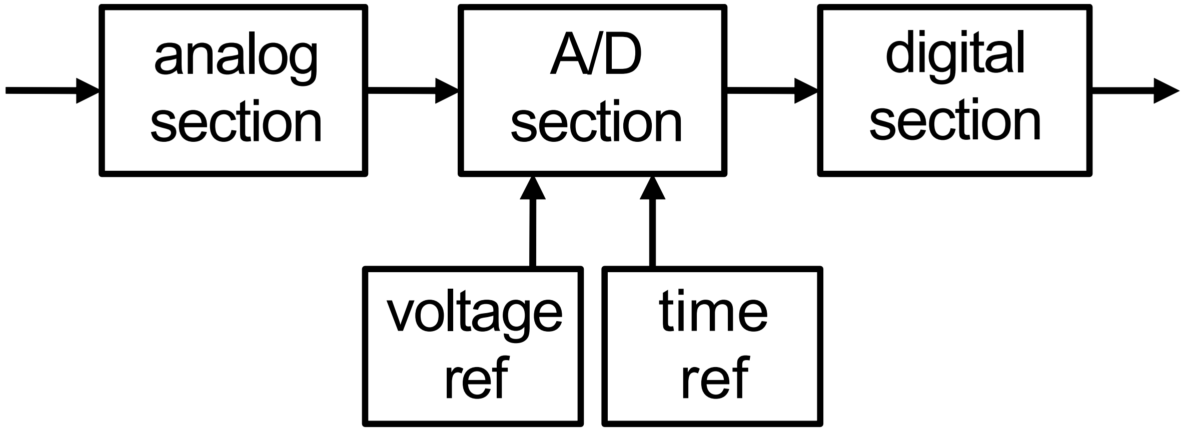
DAS:

GENERAL ARCHITECTURE

DAS general architecture

rational use of DAS requires to know its general **architecture**, **characteristics** and **performance** of adopted technologies

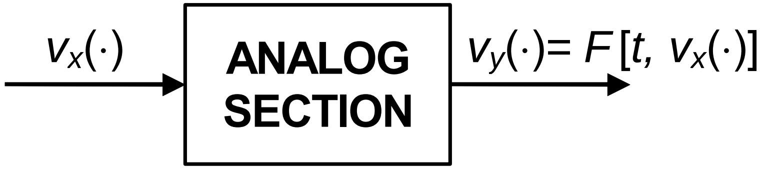
3 **sections** can be distinguished:



DAS:

ANALOG SECTION

Analog section: main characteristics



resolution
theoretically infinite

values defined on the real axis

quantity of **information** carried by signals is **finite**

sensitivity to:
- **tolerances** of the production process
- **environmental factors** (T, V_{supply}, t, ...)
- **noise** (voltages corrupting the useful signal)
  - internal (thermal, shot, flicker, ...)
  - external (interferences generated by other circuits)

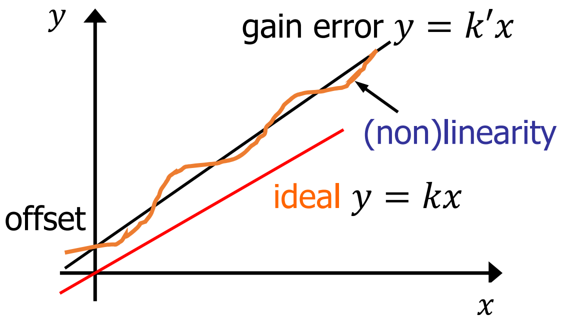
processing:
- low flexibility (programming is difficult)
- high speed (limited only by propagation time)
- many operations difficult/impossible (e.g.: ordering voltages by value)

high power consumption
active devices require both voltage and current

poor storage capability
- capacitors (fast writing, short duration)
- magnetic support (slow writing, long duration)

poor insulation capability
achieved using magnetic transformers

Analog section: performance parameters



output accuracy:

static: slowly varying input signals
(max input frequency $\ll$ analog section bandwidth)

parameters:
offset, gain error, linearity, …
sensitivity to noise
sensitivity to environmental factors,

dynamic: quickly varying input signals
(max input frequency $\geq$ analog section bandwidth)

analog section modelled as a **linear systems** (**filters**)

parameters:
bandwidth, rise-time, delay, …

signal **transformations** are possibly performed by **digital section** due to its (usually) **superior performances**

full analog systems are often employed for:

- signal with GHz bandwidth (due to ADC speed limit)
- high power systems (digital components require low voltage signals)
- very high processing speed
- very low cost systems

DAS:

DIGITAL SECTION

Digital section: characteristics

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$$x[\cdot] \longrightarrow \boxed{\text{DIGITAL SECTION}} \longrightarrow y[\cdot] = F(t, x[\cdot])$$

digital technology **overcome** many drawbacks of analog technology

immunity
- to tolerances
- noise
- environmental factors

thanks to signal regeneration

low power consumption

voltage of current are negligible in static conditions

high processing flexibility

high insulation capability

thanks to optical couplers

high transmission performance

limits:
- **finite resolution** (false problem)
- **high bandwidth** signals (GHz)
- **high power systems** (digital components require low voltage signals)
- **processing speed** can be **low** (processing algorithms = sequence of basic operators)

to understand **digital section performance**, basic knowledge of **digital signal processing** is useful

Signal processing: basic concepts

for simplicity, quantization is neglected
(signals values are on the real axis)

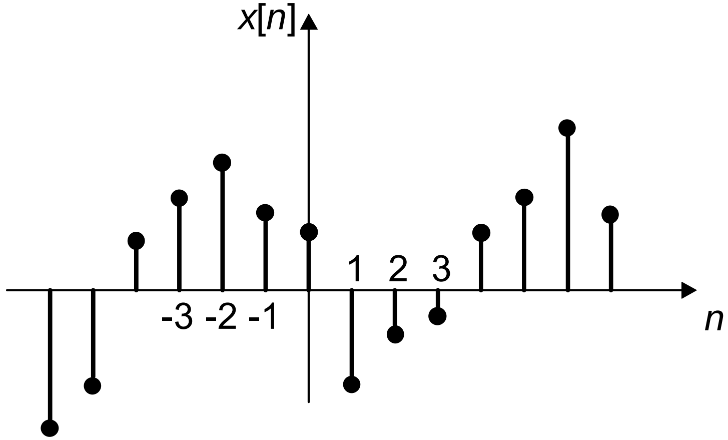
discrete time signals often derived from analog signals by **sampling**

signal defined in a discrete set $\{t_n, -\infty < n < +\infty\}$

uniform sampling is often adopted: $t_n = n\,T_s + t_0$

sampling rate $F_s = \dfrac{1}{T_s}$
[sample/s]

sampling period
(constant)



for simplicity T_s is assumed equal to 1
time is **identified** with the integer n

discrete time signal described by a **sequence**: $x[\cdot] = \{x[n]\} \quad -\infty < n < +\infty$

acquired data are stored in memory

one-to-one map:
memory address $\leftrightarrow$ sampling instant

n may represents **memory address** where the sample is stored

Signal processing: basic concepts

FUNDAMENTAL THEOREM OF SAMPLING (Nyquist - Shannon)

an analog signal with max frequency B_x (**bandwidth**) is **completely determined** by its samples taken with a sampling rate $F_s \geq 2B_x$

no loss of information due to sampling

a formula is available to **reconstruct** the analog signal from its samples

Nyquist rate: minimum (theoretical) sampling rate = $2\ B_x$

in practice $F_s > 2.5 \div 3\ B_x$ at least

Sequential processing

an **output sample** is provided **every new input sample** (e.g., **digital filtering**)

a simple **example**: M samples **moving average** (**low pass filter**)

direct implementation

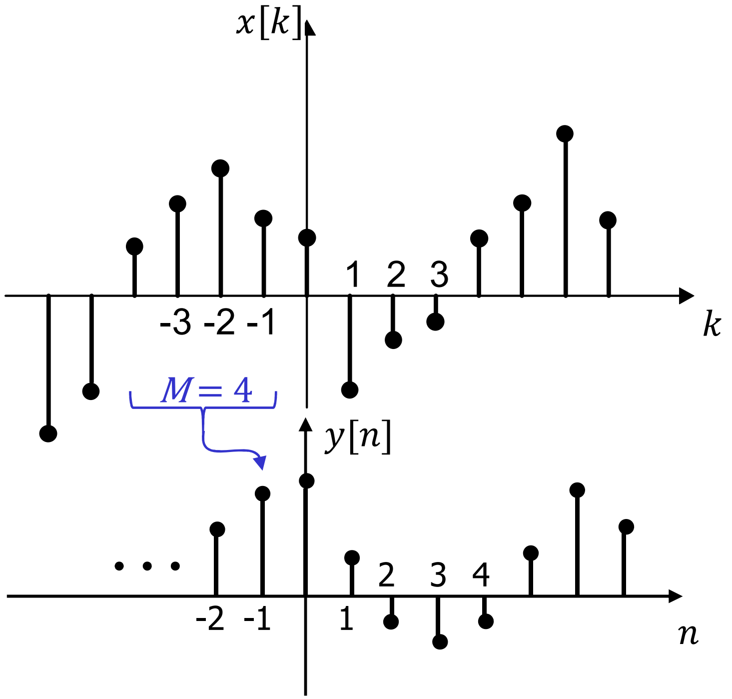
$$y[n] = \frac{1}{M}\sum_{k=0}^{M-1} x[n-k]$$

needed computation:
$(M-1)$ memory locations
$(M-1)$ + , 1 ×

recursive implementation

$$y[n] - y[n-1] = \frac{1}{M}\left(x[n] - x[n-M]\right)$$

needed computation :
$(M+1)$ memory locations
2 + , 1 ×



Block (or record) processing

output samples are provided **every** N **new input samples**

a common **example**: **Discrete Fourier Transform** (**DFT**)

DFT is used to compute an approximated signal spectrum

DFT direct formula:

$$X[k] = \frac{1}{N} \sum_{n=0}^{N-1} x[n] e^{-j\frac{2\pi}{N}nk} \qquad k = 0, 1, \dots, N-1$$

DFT inverse formula:

$$x[n] = \frac{1}{N} \sum_{k=0}^{N-1} X[k] e^{+j\frac{2\pi}{N}nk} \qquad n = 0, 1, \dots, N-1$$

Digital section: performance parameters

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- **throughput rate**: output updating rate [sample/s]
- (output) **latency**: delay between input variation and related output variation [s]
- (output) **accuracy** depends on:
  - quantization of computation
  - output sensitivity to input noise

processing can be:

ON-LINE: data are processed **as soon as available**

OFF-LINE: data are **stored** and **later processed**

for an amount of time

REAL-TIME processing = **on-line** processing ensuring

processing rate ≥ data acquisition rate

for sequential processing:

$$T_{prc} < T_s$$

processing time, sampling period

input information can be **processed without interruption** due to finite acquisition memory length

Digital section: performance parameters

(processing) **real-time bandwidth** $RTBW$:

max allowed frequency B_x for a signal to be **processed in real-time** when sampled at **Nyquist rate** ($F_s = 2B_x$)

SEQUENTIAL processing:

processing time

latency = T_{prc} [s]

throughput $= \dfrac{1}{T_{prc}}$ [sample/s]

real-time processing if $T_{prc} < T_s$

$$RTBW = \frac{1}{2T_{prc}}$$

BLOCK processing:

processing time from the last sample of the input block

latency = T_{prc} [s]

throughput $= \dfrac{N}{T_{prc}}$ [sample/s]

real-time processing if $T_{prc} < T_s$

$$RTBW = \frac{N}{2T_{prc}}$$

if $B_x > RTBW$, the **information** associated to input analog signal is **preserved** if:

- sampling: $T_s < 1/(2B_x)$
- storing: $T_{mem} < T_s$

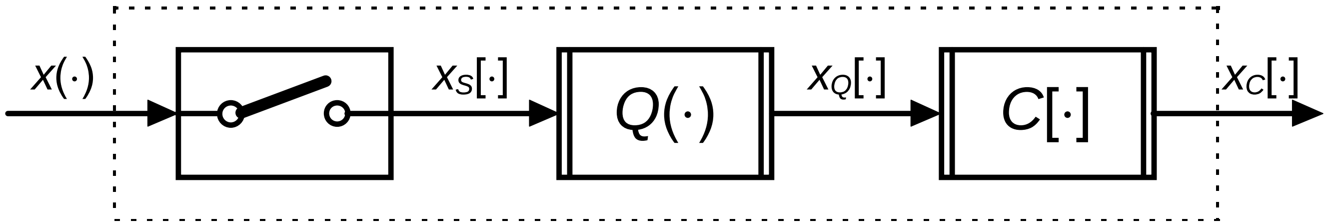
then data can be processed **off-line**

when memory is full, acquisition must be interrupted

DAS:
A/D SECTION

A/D section transformations

A/D section



sampling

(time discretization)

$$x(\cdot) \rightarrow x_S[\cdot]$$

uniform: samples equally spaced in time

$$F_S = \frac{1}{T_S}$$

sampling rate

T_S sampling period

$$x_S[\cdot] = \{x(nT_S), n = \dots -1, 0, 1, \dots\}$$

sampled signal

quantization

(value discretization)

$$x_S[\cdot] \rightarrow x_Q[\cdot]$$

discrete time and discrete values (digital signal)

encoding

(numerical representation of quantized values)

$$x_Q[\cdot] \rightarrow x_C[\cdot]$$

in a given base (usually binary)

A/D section components

sampling-and-hold amplifier
sampling implementation

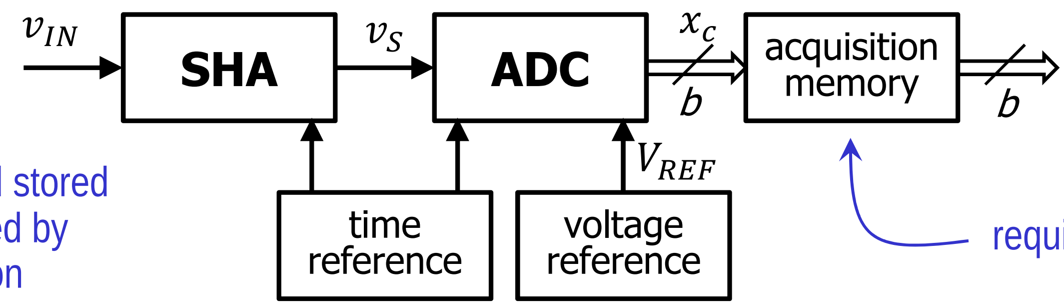
analog-to-digital converter
quantization and coding implementation

constant (**slowly-varying**) signal v_S is **quantized** by **comparison with reference** V_{REF}

quantized value is then **encoded** (usually in base

$$x_c = \frac{v_S}{V_{REF}}$$

expressed using b bits



v_{IN} is sampled and stored over time required by A/D conversion

if v_{IN} is **slowly varying** then SHA is not required

variations during conversion time < ADC resolution (LSB)

a **common clock** to synchronize:
- sampling, holding of SHA
- start, end of A/D conversion

clock period can be changed via HW or SW

required by high speed **high speed** ADC
not necessary if F_S <
data transfer rate to system memory

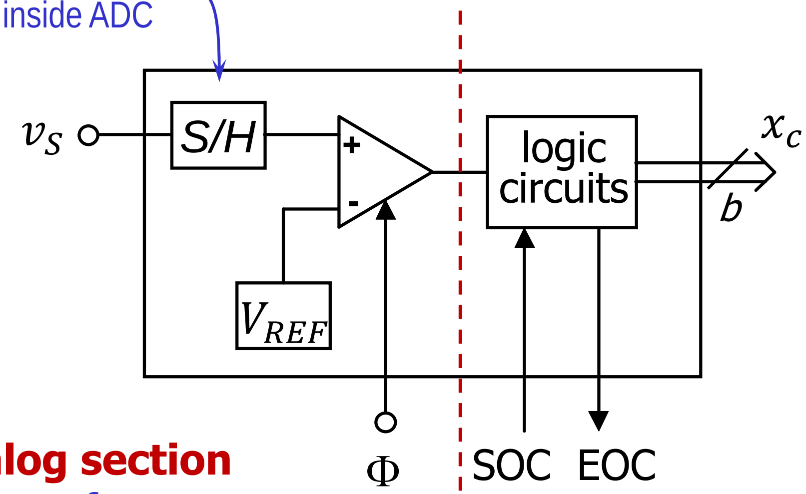
ADC general structure

ADC is the **interface** between **analog section** and **digital section**

it is often the **bottleneck** of **system performance** in terms of both:

- **conversion rate** F_{ADC}
- **accuracy** (related to number of bits b)

sometimes inside ADC



clock

analog section

- voltage reference
- clocked comparators
- S/H circuitry

logic output: 0, 1

digital section

- control logic
- digital buffer (b bits)

ADCs: main families

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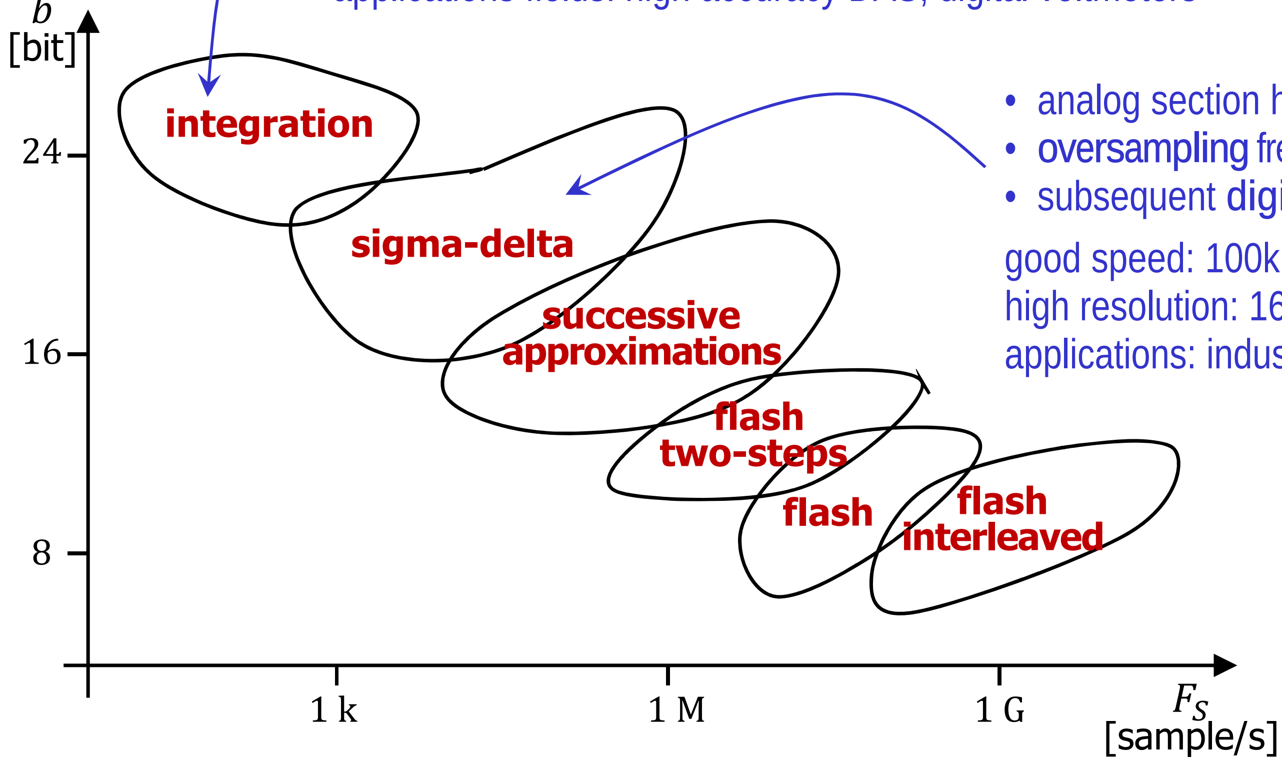
velocity – accuracy tradeoff: a qualitative relationship

waveform average value (in a given interval) is digitized
low speed: 10-1000 Sa/s
very high resolution: 20-30 bit
applications fields: high accuracy DAS, digital voltmeters

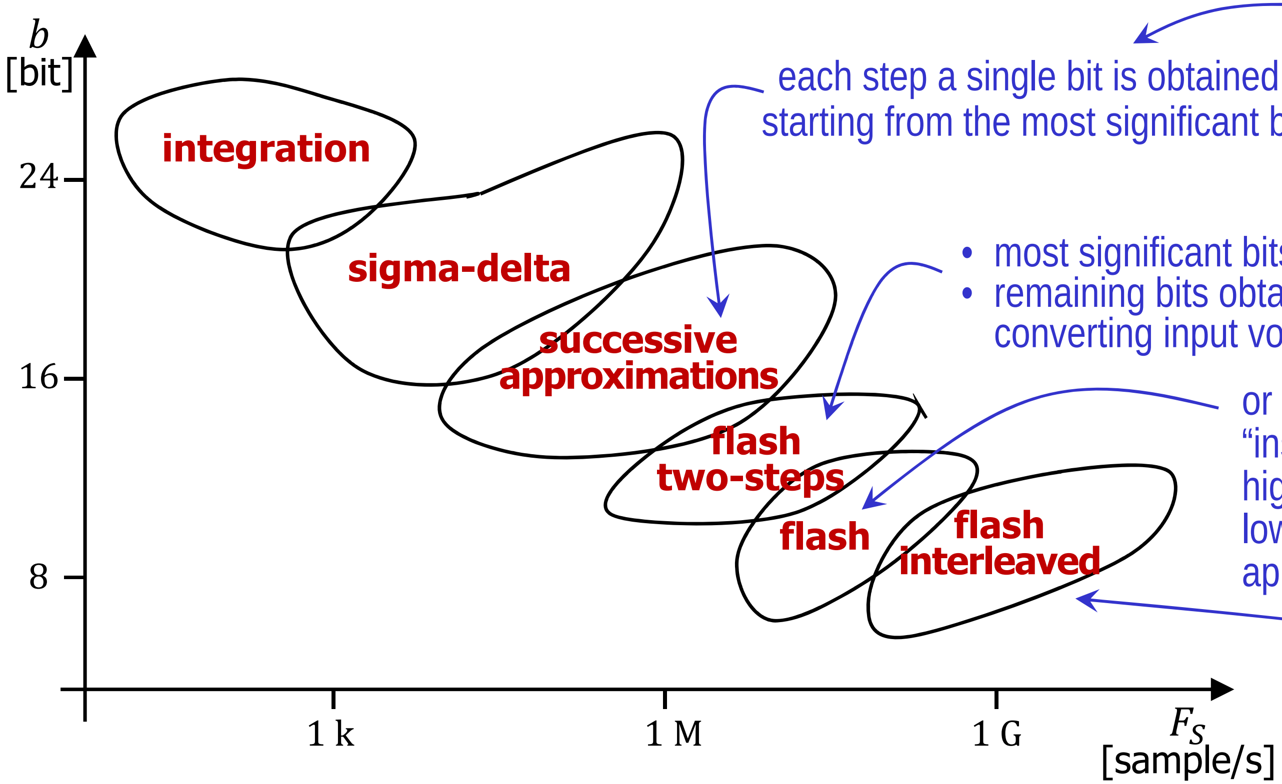
complexity of analog section minimized, strong integration, low cost, low power consumption

- analog section has **one/few comparators**: provides one/ few bits
- **oversampling** frequency; quantization **noise shaped** due to feedbacks
- subsequent **digital filtering** allows to achieve a high resolution

good speed: 100k -10M Sa/s
high resolution: 16-24 bit
applications: industrial DAS, digital voltmeters, communications



ADCs: main families



each step a single bit is obtained, starting from the most significant bit

multi-step ADCs:
more conversion steps: SHA can be needed
good speed ~ 1 -100 MSa/s
good resolution: 12-16 bit
application fields: industrial DAS

- most significant bits obtained with 1st step
- remaining bits obtained with 2nd step converting input voltage minus result of 1st step

or parallel ADCs:
“instantaneous” conversion: SHA often not required
high speed ~1 GSa/s
low resolution: 6-10 bit
application fields: digital scopes

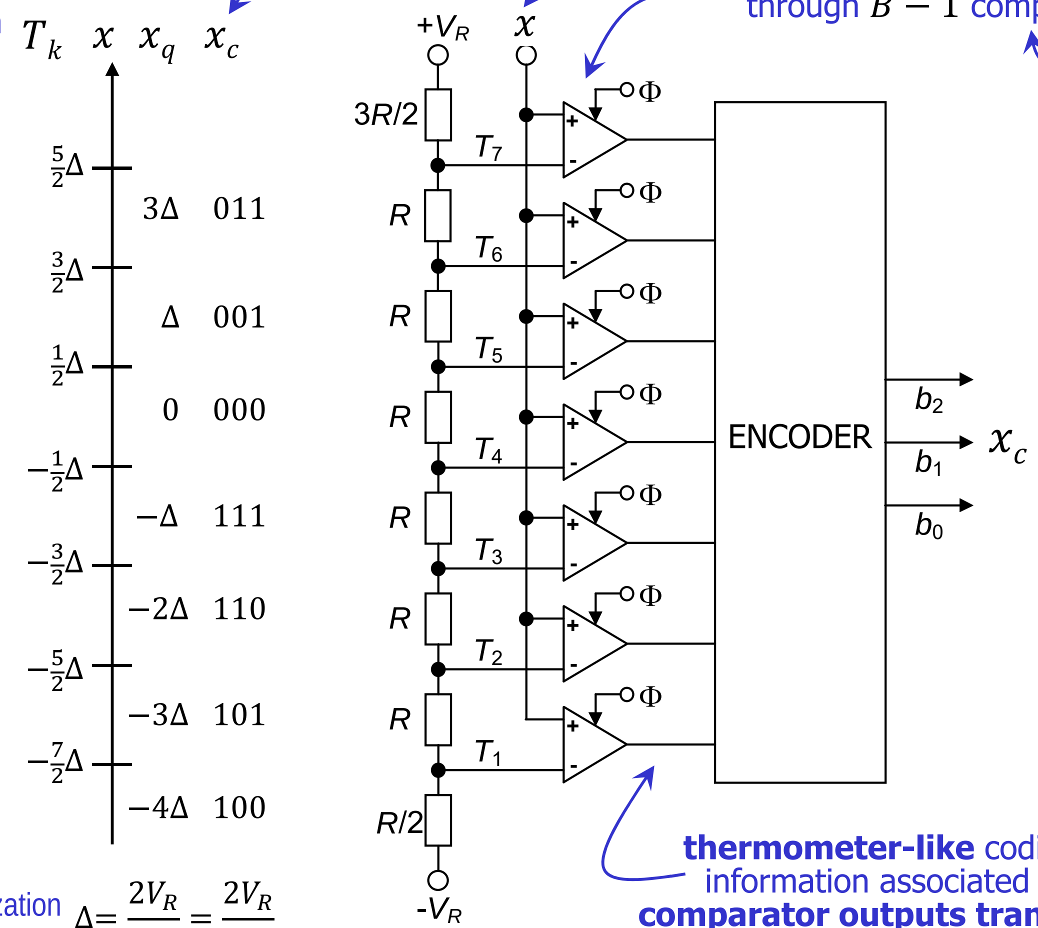
more flash ADC multiplexed
very high speed ~1 - 10 GSa/s
low resolution: 6-10 bit
application fields: top-level digital scopes

Flash ADCs

two complement code

input voltage

quantization thresholds



quantization step $\Delta = \dfrac{2V_R}{B} = \dfrac{2V_R}{8}$

quantization implemented through $B-1$ comparators $\quad B = 2^b$

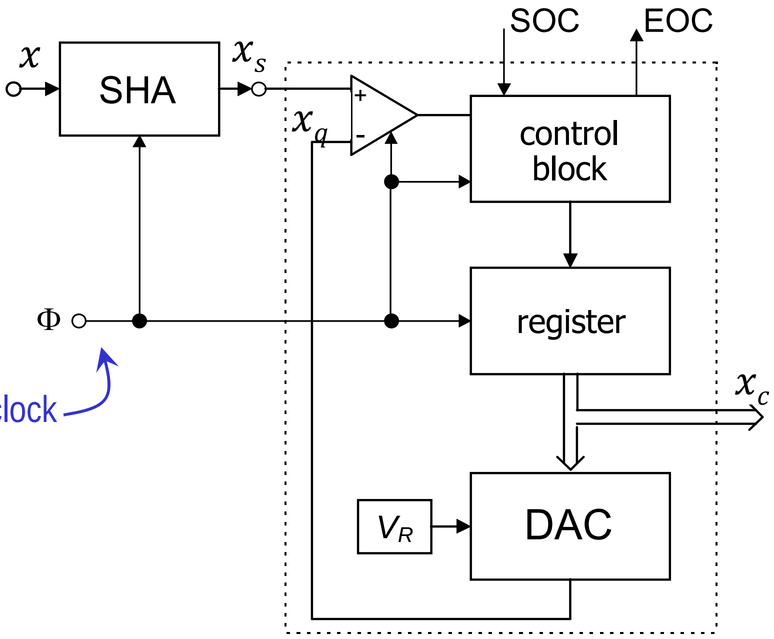
simultaneous quantization and encoding: digits of $x_c[\cdot]$ are obtained directly from $x[\cdot]$ (without generating $x_q[\cdot]$)

ADC output provided in b**-bit binary code**

thermometer-like coding: information associated to **comparator outputs transition** (non-positional notation)

two adjacent comparators exhibit opposite logic level outputs

Successive approximation ADCs

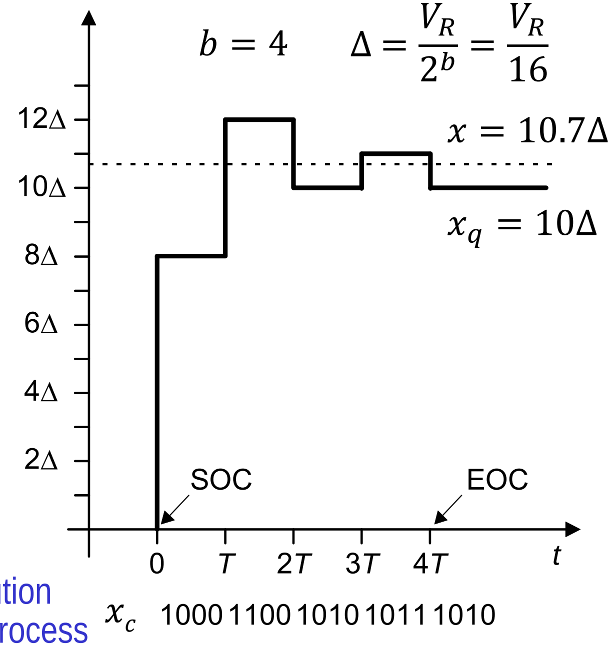


A conversion procedure:

SOC
all bits $= 0$ ** initialization
for $n = 1 \dots b$ ** the cycle start form the most significant bit
  when (active transition of) clock do
    $b(n) \leftarrow 1$ ** analyzed bit
    determine sign of $x_s - x_q$
    if $x_s - x_q > 0$
    then $b(n) \leftarrow 1$ ** bit confirmed
    else $b(n) \leftarrow 1$
  endwhen
endfor
EOC ** register contains x_c

$$T_{ADC} = b\,T_1$$

time needed for a single bit conversion

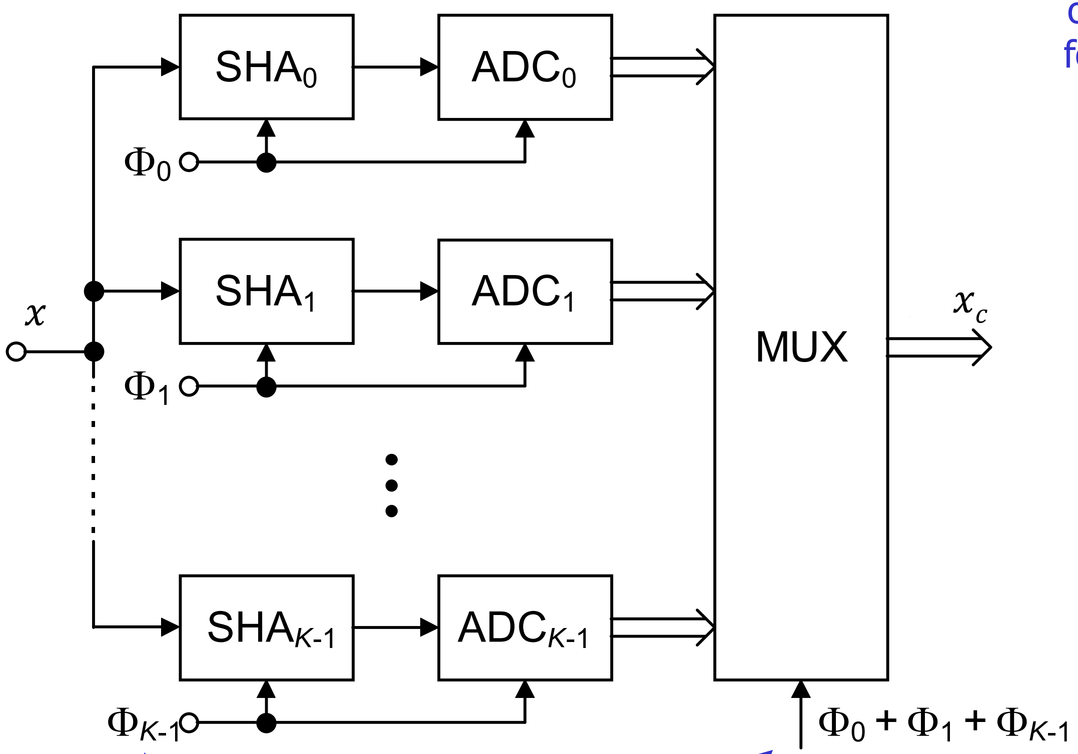


ADC output x_c evolution during the conversion process

Interleaved (flash) ADCs

$K = 2^k$ flash ADCs interleaved

digital multiplexer selects one of the K inputs and forwards it at the output



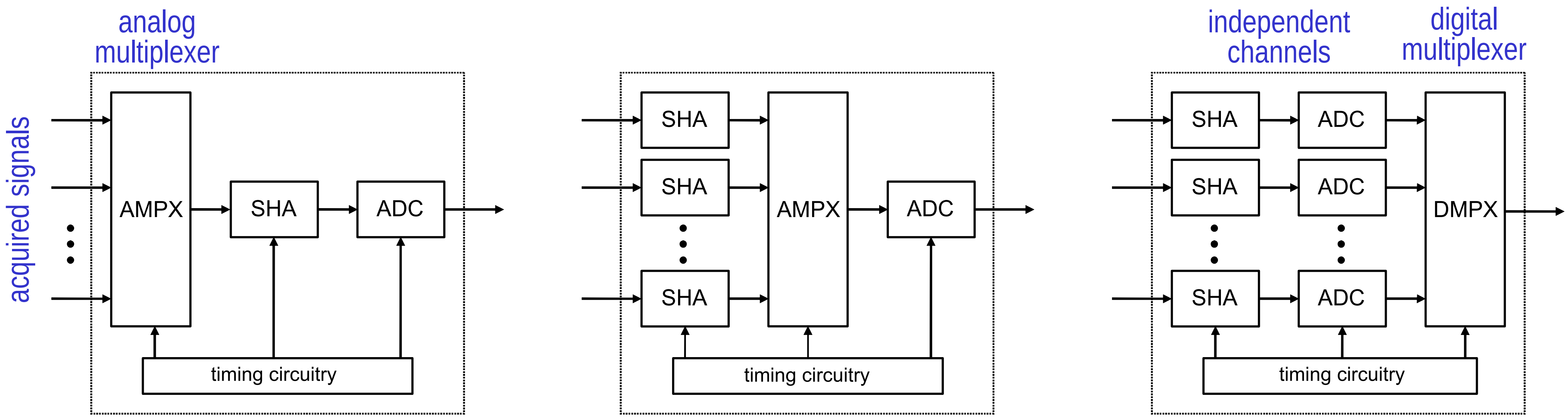
clocks

k MUX selection inputs

$$F_{ADC} = K \cdot F_s$$

single ADC sample rate

Multichannel A/D Section



- min circuit complexity
- channels are sampled one at a time
- SHA input change rapidly even with slowing varying input signals
- programmable gain amplifier could take place after AMPX

- input signals sampled simultaneously thus preserving time relations
- SHA not required for slowly-varying input signals

- min probability of failure (max reliability)
- reduced ADC sampling rate
- SHA not required for slowly-varying input signals
- distortions due to AMPX commutations avoided

optimal solution depends on price, accuracy, reliability, …

A/D Section: performance parameters

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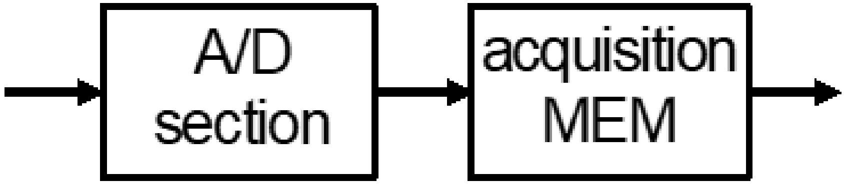
usually 3 dB bandwidth

analog bandwidth
B_3 of A/D input circuitry

in a digitizer also the
analog section bandwidth
must be considered



max record length N_A:
max n° of storable samples
= acquisition memory size

required by high speed **high speed** ADC

not necessary if F_S <
data transfer rate to system memory

conversion rate F_{ADC} :
max allowed sampling rate F_s

n° of **resolution bits** b

accuracy parameter of A/D section

n° of **effective bits** b_E
(or **significant bits**):
bits containing information
on input signal

can be **estimated** by feeding the DAS with a full-scale amplitude sinewave; sinewave parameters are estimated by fitting output samples (e.g., using least squares) and evaluating the residual;

b_E is the determined from the sinewave power to residual power ratio

other accuracy parameters can be defined, such as
signal to noise and distortion ratio (SINAD),
total harmonic distortion (THD),
spurious free dynamic range (SFDR)

depends on sinewave **frequency**
(e.g. because of sampling jitter)